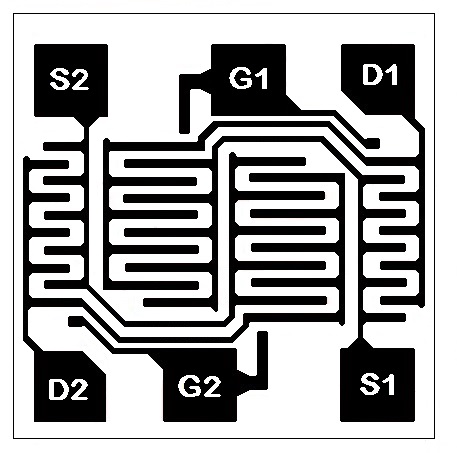
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.028”**

**.027”**



**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: CJ2**

**APPROVED BY: DK DIE SIZE .027” X .028” DATE: 5/12/16**

**MFG: CALOGIC THICKNESS .008” P/N: XDPAD1**

**DG 10.1.2**

#### Rev B, 7/1